EXERCISE: What are the new W/L ratios for the transistors in Ex. 6.7 if $V_{TOL} = -1.5$ V?

ANSWERS: $(W/L)_S = 1.17/1; (W/L)_L = 1/1.72$

### 6.6.4 STATIC DESIGN OF THE PSEUDO NMOS INVERTER

It is also possible to replace the load resistor with a PMOS transistor with its source connected to $V_{DD}$, its drain is connected to the output node, and its gate connected to ground, as in Fig. 6.24. This circuit has become known as pseudo NMOS since circuit operation is very similar to that of NMOS logic even though it is usually found embedded in CMOS designs that we will study in detail in Chapter 7.

In order to design the circuit, we use the same circuit conditions that were used for the case of the resistive load. $(i_{DD} = 80 \mu$A, $V_{DD} = 2.5$ V and $V_L = 0.20$ V). First, we choose the $W/L$ ratio of the PMOS load device to limit the operating current in the inverter. Then we calculate the size of $M_S$ required to achieve the specified value of $V_L$. (Note that neither transistor suffers from any body effect since the bulk terminals of both transistors are connected to their respective sources. This is an important advantage of the PMOS load transistor in comparison to NMOS load devices.)

#### Calculation of $(W/L)_P$ and $(W/L)_S$

For the PMOS device in Fig. 6.24, we see that $V_{GS} = -V_{DD}$, and the transistor will be in the conducting state. Since $V_{DS} = 0.2 - 2.5 = -2.3$ V and $V_{GS} - V_{TP} = -2.5 - (-0.6) = -1.9$ V, the transistor will be saturated ($|V_{DS}| > |V_{GS} - V_{TP}|$—see Section 4.2). We need to find the value of $W/L$ that sets the PMOS drain current to 80 $\mu$A:

$$i_D = \frac{K'_D}{2} \left( \frac{W}{L} \right)_P (V_{GS} - V_{TP})^2$$

or

$$80 \mu$A = \frac{1}{2} \left( \frac{40 \mu$A}{V^2} \right) \left( \frac{W}{L} \right)_P [-2.5 - (-0.6)]^2 V^2$$

which gives

$$\left( \frac{W}{L} \right)_P = \frac{1.11}{1}$$

#### Calculation of $V_H$ and $(W/L)_S$

In order to calculate $(W/L)_S$, we need to determine the high output level $V_H$, since this is the voltage that is used to drive switching transistor $M_S$ to achieve $v_o = V_L$. As shown in Fig. 6.24(b), the PMOS load transistor has a fixed value of $V_{GS} = -2.5$ V. Thus it will always be in the conducting state. With $M_S$ off, current will flow through the PMOS device to charge the output node until the drain-source voltage $V_{DS}$ of the transistor collapses to zero. Thus, $V_H = V_{DD}$, just as for the inverter with the resistor load.

Now, the conditions for switching transistor $M_S$ with $v_o = V_L$ in Fig. 6.24(a) are $V_{GS} = V_H = 2.5$ V and $V_{DS} = V_L = 0.20$ V with $i_D = 80$ $\mu$A. These are identical to those of the switching

![Figure 6.24 Pseudo NMOS Inverter with (a) $v_I = V_H$ and (b) $v_I = V_L$.]
transistor in the resistor load inverter in Section 6.5.2. Thus, \((W/L)_S = 2.22/1\). The completed pseudo NMOS inverter design appears in Fig. 6.25.

**EXERCISE:** Verify the value of \((W/L)_S\) by calculating the drain current of \(M_9\).

**EXAMPLE 6.8 LOGIC LEVEL ANALYSIS FOR THE PSEUDO NMOS INVERTER**

Finding the logic levels associated with someone else’s inverter design involves a different thought process than that required to design the inverter. Here we find \(V_H\) and \(V_L\) for a specified inverter design.

**PROBLEM** Find the high and low logic levels and the power supply current for the pseudo NMOS inverter in Fig. 6.26 with \((W/L)_N = 10/1\) and \((W/L)_L = 2/1\). The inverter operates with \(V_{DD} = 2.5\) V. Assume \(K'_n = 100\ \mu\text{A/V}^2\), \(V_{FN} = 0.60\) V, \(K'_p = 40\ \mu\text{A/V}^2\), \(V_{FP} = -0.60\) V.

**SOLUTION** Known Information and Given Data: Circuit topology in Fig. 6.26: \(V_{DD} = 2.5\) V, \((W/L)_N = 10/1\), \((W/L)_L = 2/1\), \(K'_n = 100\ \mu\text{A/V}^2\), \(V_{FN} = 0.60\) V, \(K'_p = 40\ \mu\text{A/V}^2\), and \(V_{FP} = -0.60\) V.

**Unknowns:** \(V_H, V_L, I_{DD}\) for both logic states

**Approach:** First determine \(V_H\). Use \(V_H\) and the specified transistor parameters to find \(V_L\) by equating the drain currents in the switching and load transistors. Use \(V_L\) to find power supply current \(I_{DD}\) which is equal to switching transistor drain current \(I_{DS}\).

**Assumptions:** \(M_9\) is off for \(V_I = V_L\). For \(V_O = V_L\), \(M_5\) operates in the triode region, and \(M_L\) is in the saturation region.

**Analysis:** First we find \(V_H\), and then we use it to find \(V_L\). For the pseudo NMOS logic gate, \(V_H = V_{DD}\). Thus, for our circuit, \(V_H = 2.5\) V. To find \(V_L\), we use the condition that the two transistor drain currents must be equal in the steady state: \(I_{DS} = I_{DL}\). For \(V_O = V_L\), we expect that the load transistor will be saturated since the magnitude of its drain-source voltage is large (\(V_{DS} = V_L - V_{DD}\)), and we expect the switching transistor to be in the triode region since its drain-source voltage will be small. (\(V_{DS} = V_L\).) For \(I_{DS} = I_{DL}\), we have

\[
K'_n \left( \frac{10}{1} \right) \left( V_{GSN} - V_{FN} - \frac{V_L}{2} \right) V_L = \frac{K'_p}{2} \left( \frac{2}{1} \right) (V_{GSP} - V_{FP})^2
\]

For the circuit in Fig. 6.24, \(V_{GSN} = 2.5\) V and \(V_{GSP} = -2.5\) V, and

\[
\frac{100\ \mu\text{A}}{V^2} \left( \frac{10}{1} \right) \left( 2.5 - 0.6 - \frac{V_L}{2} \right) V_L = \frac{40\ \mu\text{A}}{2\ V^2} \left( \frac{2}{1} \right) (-2.5 - (-0.6))^2
\]
which can be rearranged to yield a quadratic equation:

\[ 12.5v_L^2 - 47.5v_L + 3.61 = 0 \]

for which \( v_L = 0.0776 \text{ V}, 3.72 \text{ V}. \)

\( V_L = 3.72 \text{ V} \) exceeds the 2.5-V power supply, so that answer must be discarded. Hence the answer must be \( v_L = 0.0776 \text{ V}. \) For this value of \( v_L, \) the current in \( M_S \) is

\[ I_{DS} = \left( \frac{100 \mu A}{V^2} \right) \left( \frac{10}{1} \right) \left( 2.5 - 0.6 - \frac{0.0776}{2} \right) (0.0776)^2 = 144 \mu A \]

**Check of Results:** For \( v_L, \) we should check our triode and saturation region assumptions for the two MOSFETs: For the switching transistor, \( V_{GS} - V_{TH} = 2.5 - 0.6 = 1.90 \text{ V} \) which is greater than \( V_{DS} = 0.078 \text{ V}, \) and the triode region assumption is correct. For the load device, \( V_{GS} - V_{TH} = -2.5 - (-0.6) = -1.9 \text{ V}, \) and \( V_{DS} = 0.078 - 2.5 = -2.42, \) which are consistent with the saturation region of operation. We can further check our results by finding the drain current in \( M_L: \)

\[ I_{DL} = \left( \frac{40 \mu A}{2 V^2} \right) \left( \frac{2}{1} \right) (-2.5 + 0.6)^2 = 144 \mu A \]

which agrees with \( I_{DS}. \)

**Computer-Aided Analysis:** To verify our design with SPICE, we draw the circuit with a schematic capture tool. Two inverters are cascaded in order to get both \( V_H \) and \( V_L \) with one simulation. The gate of MS1 is grounded to force MS1 to be off. The NMOS transistor uses the LEVEL = 1 model with \( KP = 10E-5, \) \( VTO = 0.6 \text{ V}, \) \( GAMMA = 0.5 \text{ V}, \) and \( PHI = 0.6 \text{ V}, \) and the PMOS parameters are \( KP = 4E-5, \) \( VTO = -0.6 \text{ V}, \) \( GAMMA = 0.5 \text{ V}, \) and \( PHI = 0.6 \text{ V}. \) The transistor sizes are specified as \( W = 10 \text{ U} \) and \( L = 1 \text{ U} \) for \( M_S, \) and \( W = 2 \text{ U} \) and \( L = 1 \text{ U} \) for \( M_L. \) SPICE gives \( V_H = 2.50 \text{ V} \) and \( V_L = 0.0776 \text{ V}. \) The current in \( V_{DD} \) is 144 \( \mu A. \) All the values agree with the hand calculations.

![Circuit Diagram](image)

**EXERCISE:** Use the “Solver” in your calculator to check the value of \( V_L \) found in Section 6.7.2.

**EXERCISE:** Repeat the calculations with \( (W/L)_S = 5/1. \) Check your results with SPICE.

**ANSWERS:** 2.50 V, 0.159 V, 144 \( \mu A. \)

**Noise Margin Analysis for the Pseudo NMOS Inverter**

Let us now find the noise margins for the pseudo NMOS inverter. We need to calculate the values of \( V_{IL}, V_{OL}, V_{IH}, \) and \( V_{OH} \) and remember these voltages are defined by the points on the voltage transfer characteristic at which the slope \( dv_o/dv_i = -1, \) as indicated on the graph in Fig. 6.27.

First let us find \( V_{IL} \) and \( V_{OL}. \) We need to find a relationship between \( v_i \) and \( v_o \) that we can differentiate. Remember that the drain currents in the switching and load devices must be equal at all points on the static VTC. Also, at \( v_i = V_{IL} \) the input will be at a relatively low voltage, and the
output will be a relatively high voltage. Thus, we guess that $M_S$ will be operating in the saturation region and that $M_L$ will operate in the triode region. Setting $i_{DS} = i_{DL}$ yields

$$\frac{K_S}{2}(v_I - V_{TN})^2 = K_L \left( -V_{DD} - V_{TP} - \frac{v_O - V_{DD}}{2} \right) (v_O - V_{DD})$$

with

$$K_S = K'_S \left( \frac{W}{L} \right)_S$$

and

$$K_L = K'_L \left( \frac{W}{L} \right)_L$$

(6.29)

The point of interest is $\frac{\partial v_O}{\partial v_I} = -1$, but solving for the value of $v_O$ would be quite tedious. Since we expect the derivatives to be smooth, continuous, and nonzero, we will assume that $\frac{\partial v_O}{\partial v_I} = \left( \frac{\partial v_I}{\partial v_O} \right)^{-1}$ and solve for $v_I$ in terms of $v_O$:

$$v_I = V_{TN} + \frac{1}{\sqrt{K_R}} \sqrt{[2(V_{DD} + V_{TP}) - (V_{DD} - v_O)](V_{DD} - v_O)}$$

where $K_R = \frac{K_S}{K_L}$

Evaluating the derivative is still quite tedious, so only the results are given here:

$$V_{IL} = V_{TN} + \frac{(V_{DD} + V_{TP})}{\sqrt{K'_S + K'_R}}$$

and

$$V_{OH} = V_{DD} - (V_{DD} + V_{TP}) \left( 1 - \sqrt{\frac{K_R}{K_R + 1}} \right)$$

(6.30)

For the inverter design of Fig. 6.26 with $V_{DD} = 2.5$ V, $V_{TP} = -0.6$ V and $K_R = (2.22)(100)/(1.11)(40) = 5$, we find

$$V_{IL} = 0.6 + \frac{(2.5 - 0.6)}{\sqrt{(5)^2 + 5}} = 0.95 \text{ V}$$

and

$$V_{OH} = 2.5 - (2.5 - 0.6) \left( 1 - \sqrt{\frac{5}{5 + 1}} \right) = 2.33 \text{ V}$$

These values appear reasonable. The input must exceed the threshold voltage of the NMOS transistor before it begins to conduct, so $V_{IH}$ will be somewhat larger than $V_{TN}$, and the value of $V_{OH}$ should be somewhat below $V_{DD}$ as in Fig. 6.27.

With these values we can check our assumptions of the operating regions of $M_S$ and $M_L$. For the NMOS switching transistor, $V_{GS} - V_{TN} = 0.95 - 0.6 = 0.35$ V and $V_{DS} = 2.33$ V. Since $V_{DS} > V_{GS} - V_{TN}$, the saturation region assumption was correct. For the PMOS load device, $V_{GS} - V_{TP} = -2.5 - (-0.6) = -1.9$ V and $V_{DS} = 2.33 - 2.5 = -0.17$ V. Since the magnitude of $V_{DS}$ is less than that of $V_{GS} - V_{TP}$, the triode region assumption was correct.

A similar process is used to find $V_{ih}$ and $V_{oh}$. We again observe that the drain currents in the switching and load devices must be equal. At $v_I = V_{IH}$, the input will be at a relatively high voltage, and the output will be at a relatively low voltage. Thus, we guess that $M_S$ will operate in the triode region and $M_L$ will be in the saturation region. Equating drain currents in the switching and load transistors yields

$$K_S \left( v_I - V_{TN} - \frac{v_O}{2} \right) v_O = \frac{K_L}{2} \left( -V_{DD} - V_{TP} \right)^2$$

(6.31)

We again assume that $\frac{\partial v_O}{\partial v_I} = \left( \frac{\partial v_I}{\partial v_O} \right)^{-1}$ and solve for $v_I$ in terms of $v_O$:

$$v_I = V_{TN} + \frac{v_O}{2} + \frac{(V_{DD} + V_{TP})^2}{2K_R} \left( \frac{1}{v_O} \right)$$

where $K_R = \frac{K_S}{K_L}$

(6.32)

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4 The details of the derivation can be found on the MCD website.
6.7 NMOS Inverter Summary and Comparison

Figure 6.27 PSPICE simulation of the voltage transfer function for the pseudo NMOS inverter.

Figure 6.28 Noise margins versus transconductance ratio $K_R$ for the pseudo NMOS inverter with $V_{DD} = 2.5$ V, $V_{SS} = 0.6$ V and $V_{PP} = -0.6$ V.

Taking the derivative

$$\frac{\partial V_I}{\partial V_O} = \frac{1}{2} - \frac{1}{2K_R} \frac{(V_{DD} + V_{TP})^2}{V_{OL}^2}$$

and setting it equal to $-1$ at $V_O = V_{OL}$ yields

$$-1 = \frac{1}{2} - \frac{1}{2K_R} \frac{(V_{DD} + V_{TP})^2}{V_{OL}^2} \quad \text{or} \quad V_{OL} = \frac{V_{DD} + V_{TP}}{\sqrt{3K_R}}$$

Substituting this result in Eq. (6.32) with $V_I = V_{IH}$ gives

$$V_{IH} = V_{TN} + \frac{2(V_{DD} + V_{TP})}{\sqrt{3K_R}} = V_{TN} + 2V_{OL}$$

(6.34)

For the inverter design of Fig. 6.26,

$$V_{OL} = \frac{V_{DD} + V_{TP}}{\sqrt{3K_R}} = \frac{2.5 - 0.6}{\sqrt{3(5)}} = 0.491 \text{ V} \quad \text{and} \quad V_{IH} = 0.6 + 2(0.49) = 1.58 \text{ V}$$

(6.35)

With these values we should again check our assumptions of the operating regions of $M_S$ and $M_L$.

For the NMOS switching transistor, $V_{GS} - V_{TN} = 1.58 - 0.6 = 0.98 \text{ V}$ and $V_{DS} = 0.491 \text{ V}$. Since $V_{DS} < V_{GS} - V_{TN}$, the triode region assumption was correct. For the PMOS load device, $V_{GS} - V_{TP} = -2.5 - (-0.6) = -1.9 \text{ V}$ and $V_{DS} = 0.491 - 2.5 = -2.01 \text{ V}$. Since the magnitude of $V_{DS}$ exceeds that of $V_{GS} - V_{TP}$, the saturation region assumption was correct. In Fig. 6.27, it can be seen that these calculated values of $V_{IL}$, $V_{OL}$, $V_{IH}$ and $V_{OH}$ all agree well with SPICE simulation results.

The noise margins for this pseudo NMOS inverter are

$$\text{NM}_{IH} = V_{OH} - V_{IH} = 2.33 - 1.58 = 0.75 \text{ V}$$

$$\text{NM}_{IL} = V_{IH} - V_{OL} = 0.95 - 0.49 = 0.46 \text{ V}$$

With Eqs. (6.30)–(6.35), we can easily explore the dependence of the noise margins on transconductance ratio $K_R$, and the results are plotted in Fig. 6.28. High-state noise margin $\text{NM}_{IH}$ increases monotonically as the drive capacity of switching transistor $M_S$, and hence $K_R$, increases, whereas $\text{NM}_{IL}$ gradually decreases.

### 6.7.1 NMOS INVERTER SUMMARY AND COMPARISON

Figure 6.29 and Table 6.6 summarize the NMOS inverter designs discussed in Secs. 6.5 and 6.6. The gate with the resistive load takes up too much area to be implemented in IC form. The saturated load configuration is the simplest circuit, using only NMOS transistors. However, it has a disadvantage