Supplement S6.3 – Delay Estimates for the NMOS Inverter with a Saturated Load

The mathematical complexity of the analysis increases for the inverters that use transistors as load elements. For hand calculations, we will obtain useful analytical results by neglecting the body effect. If more accurate estimates are needed, they can be obtained using circuit simulation with SPICE.

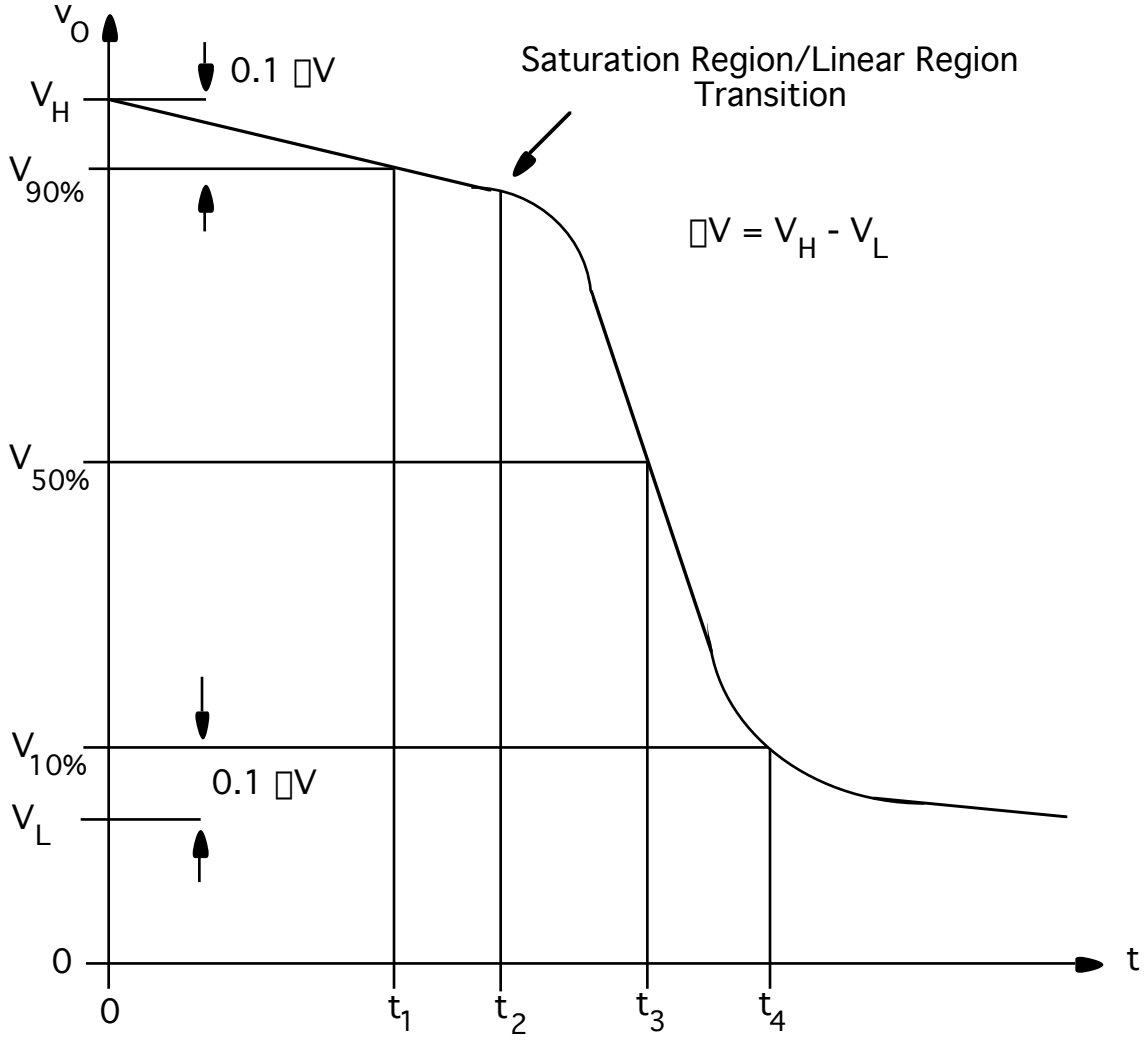

Figure S6.3.1 - The high-to-low transition for the inverter with saturated load and the times needed for calculation of τ_{PHL} and t_f. This figure is the same as Fig. 6.46 in the text , but the values associated with the various voltage levels are different.

As mentioned earlier in the text, static NMOS logic gates are "ratioed" designs, in which the current drive capability of the switching transistor must be much greater than

that of the load transistor in order to achieve a small value of V_L. Thus, we will always be able to assume that the drain current of the switching transistor is much greater than that of the load device ($i_{DS} >> i_{DL}$) during the high-to-low switching transient, except for v_O very near V_L. Therefore, we can assume that all the drain current of the NMOS transistor is available to discharge the load capacitance as in Fig. 6.44. For analysis of the saturated load inverter, the input signal v_I is assumed to be a step function changing at t = 0 reaching a value equal to $V_H = (V_{DD} - V_{TNL})$. At t = 0+, the voltage v_C on the capacitor is equal to V_H, and v_I forces $v_{GS}(0^+) = V_{DD} - V_{TNL}$.

Calculation of τ_{PHL}

The graph in Fig. S6.3.1 shows the important instants in time for this inverter. Time t_1 represents the time at which the output has dropped by 0.1 ΔV, and time t_4 is the time at which the output has dropped by 0.9 ΔV. Thus, $t_f = t_4 - t_1$. At t_3, $v_O = (V_H+V_L)/2$, so $\tau_{PHL} = t_3$. The time t_2 is also very important. At time t_2, $v_O = V_{DD} - V_{TNL} - V_{TNS}$, and the transistor changes from saturation region operation to linear region operation.

Let us focus first on calculation of τ_{PHL} and then calculate t_f. At $t = 0^+$, the NMOS switching transistor will be operating in the saturation region, and the capacitor current is

$$\frac{K_S}{2}\left(v_{GS} - V_{TNS}\right)^2 = -C\frac{dv_C}{dt}$$

$$\frac{K_S}{2}\left(V_H - V_{TNS}\right)^2 = -C\frac{dv_C}{dt} \qquad \text{(S6.3.1)}$$

in which $v_{GS} = V_H = V_{DD} - V_{TNL}$ and V_{TNS} are both constant. Thus the drain current is constant, and the capacitor discharges at a uniform rate until the MOSFET enters the linear region of operation at time t_2 when $v_C = V_H - V_{TNS}$. We see that the MOSFET enters the linear region after the capacitor voltage drops by one threshold voltage V_{TNS}.

For these values, the time required for the transistor to reach the linear region is

$$t_2 = \frac{2\,C\,V_{TNS}}{K_S\left(V_H - V_{TNS}\right)^2} = 2\,R_{ons}\,C\,\frac{V_{TNS}}{\left(V_H - V_{TNS}\right)} \tag{S6.3.2}$$

for $$R_{ons} = \frac{1}{K_S\left(V_H - V_{TNS}\right)}$$

which is the equivalent "on-resistance" of the NMOS switching transistor with $V_{GS} = V_H$ and $V_{DS} = 0$.

Once the transistor enters the linear region, the equation characterizing the discharge changes to

$$K_S\left[v_{GS} - V_{TNS} - \frac{v_C}{2}\right]v_C = -C\frac{dv_C}{dt} \tag{S6.3.3}$$

since the $v_{DS} = v_c$ for the MOSFET. Rearranging this equation with $v_{GS} = V_H$ and integrating yields

$$\int_{V_2}^{V_3} \frac{dv_C}{\left(2\left(V_H - V_{TNS}\right) - v_C\right)v_C} = \int_{t_2}^{t_3} \frac{K_S}{2C}\,dt \tag{S6.3.4}$$

in which the limits of integration are defined by

$$V_2 = v_c\,(t_2) = V_H - V_{TNS} \quad \text{and} \quad V_3 = v_c\,(t_3) = (V_H + V_L)/2\ .$$

This equation is the same as Eqn. (6.56). Using the results from Eqns. (6.58) and (6.59) yields:

$$\begin{aligned} t_3 - t_2 &= \frac{C}{K_S\left(V_H - V_{TNS}\right)}\ln\left[4\left(\frac{V_H - V_{TNS}}{V_H + V_L}\right) - 1\right] \\ &= R_{ons}\,C\,\ln\left[4\left(\frac{V_H - V_{TNS}}{V_H + V_L}\right) - 1\right] \end{aligned} \tag{S6.3.5}$$

The propagation time τ_{PHL} is just equal to t_3 and is given by

$$\tau_{PHL} = t_3 = \left(t_3 - t_2\right) + t_2 = R_{ons}\,C\left[\ln\left[4\,\frac{V_H - V_{TNS}}{V_H + V_L} - 1\right] + \frac{2V_{TNS}}{V_H - V_{TNS}}\right] \tag{S6.3.6}$$

For example, using V_{TNS} = 1 V, V_{DD} = 5 V, V_H = 3.39 V and V_L = 0.25 V, we find

$$\tau_{PHL} = R_{ons}\, C \left[\ln 4 \frac{3.39 - 1}{3.39 + 0.25}\right] \left[1 + \frac{2}{3.39 - 1}\right] = \frac{1.36\, C}{K_S\left(V_H - V_{TNS}\right)} = \frac{0.57\, C}{K_S} \qquad \text{(S6.3.7)}$$

Fall Time Calculation

The fall time is calculated from

$$t_f = t_4 - t_1 = (t_4 - t_2) - (t_2 - t_1) \ .$$

During the time interval $t_2 - t_1$, the MOSFET is saturated, and the current discharging the capacitor is constant. Therefore,

$$t_2 - t_1 = C\, \frac{\left(V_H - 0.1\,V\right) - \left(V_H - V_{TNS}\right)}{\frac{K_S}{2}\left(V_H - V_{TNS}\right)^2}$$

$$t_2 - t_1 = 2\, R_{ons}\, C \frac{V_{TNS} - 0.1\,V}{V_H - V_{TNS}} \qquad \text{(S6.3.8)}$$

During the interval $t_4 - t_2$, the MOSFET is operating in the linear region, and the circuit is again described by Eqn. (6.57):

$$\int_{V_2}^{V_3} \frac{dv_C}{\left(2\left(V_H - V_{TNS}\right) - v_C\right) v_C} = \int_{t_2}^{t_3} \frac{K_S}{2C}\, dt \qquad \text{(S6.3.9)}$$

in which the limits of integration are now given by

$$V_2 = v_c\,(t_2) = V_H - V_{TNS} \quad \text{and} \quad V_4 = v_c\,(t_3) = V_H - 0.9\,V \ .$$

Using the results from Eqn. (6.58),

$$t_4 - t_2 = R_{ons}\, C\, \ln\left[\frac{V_H - 2V_{TNS} + 0.9\,V}{V_H - 0.9\,V}\right] \quad ,$$

and our estimate for the fall time is given by:

$$t_f = t_4 - t_1 = R_{ons}\, C \left[\ln\left[\frac{V_H - 2V_{TNS} + 0.9\,V}{V_H - 0.9\,V}\right] + 2\,\frac{V_{TNS} - 0.1\,V}{V_H - V_{TNS}}\right] \qquad \text{(S6.3.10)}$$

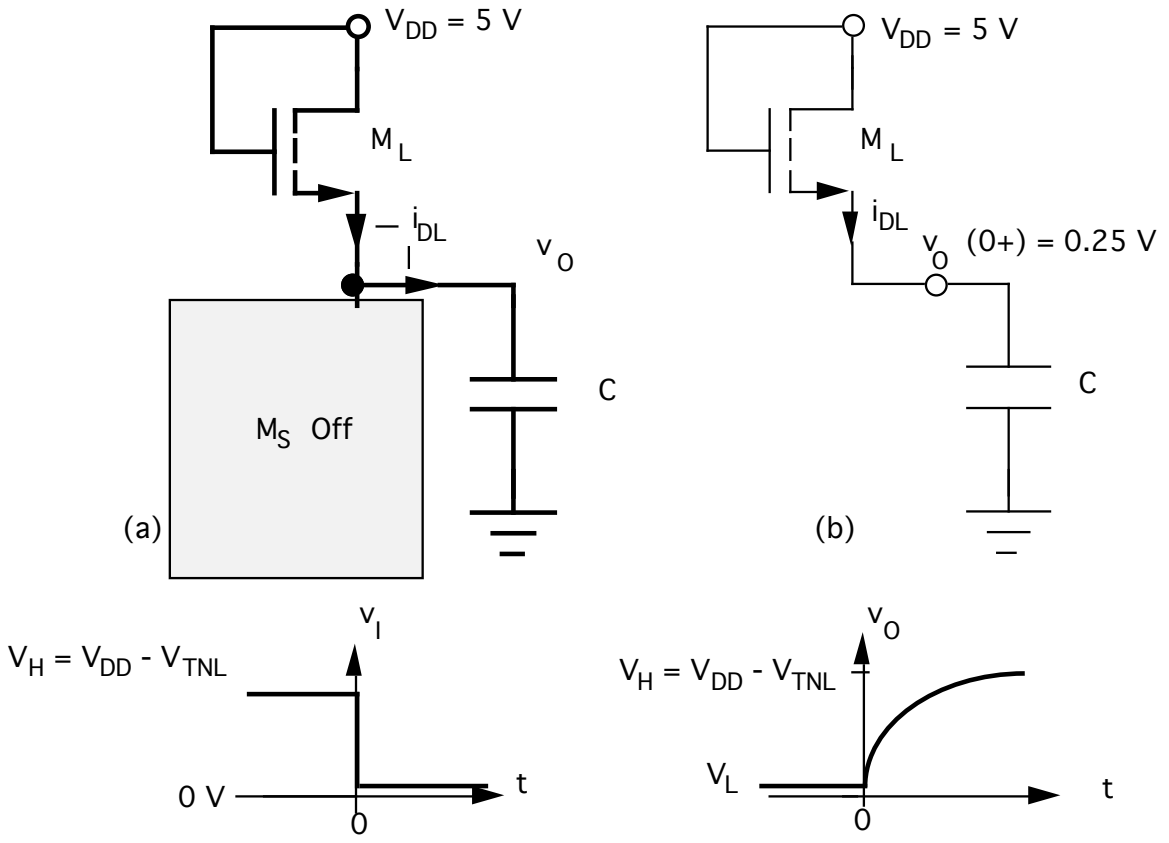

Figure S6.3.2 - Low-to-high switching transient for an inverter with a saturated load device

Calculation of τ_{PLH}

Figure S6.3.2 shows the inverter with a saturated load. At t = 0, the input signal turns off M_S. The load device is always operating in saturation, and the source current will charge the capacitor from an initial value of V_L to the final value of $V_H = V_{DD} - V_{TNL}$. The voltage at the output of the gate is governed by the following differential equation:

$$C\frac{dv_O}{dt} = i_{DL}$$

$$C\frac{dv_O}{dt} = \frac{K_L}{2}\left(V_{DD} - v_O - V_{TNL}\right)^2 \qquad \text{(S6.3.11)}$$

In order to find a solution to this equation, we will neglect the body effect in the load device and assume that the threshold voltage is constant. Letting $Z = (V_{DD} - V_{TNL} - v_O)$, Eqn. (S6.3.11) can be rewritten as

$$\frac{dZ}{Z^2} = -\frac{K_L}{2C}dt$$

which has the solution

$$\frac{K_L}{2C}t = \frac{1}{V_{DD} - V_{TNL} - v_O} + \beta.$$

Using $v_O = V_L$ at $t = 0$ allows us to determine the constant β and yields the solution we desire:

$$v_O(t) = V_{DD} - V_{TNL} - \frac{1}{\dfrac{1}{V_{DD} - V_{TNL} - V_L} + \dfrac{K_L}{2C}t} \quad . \qquad \text{(S6.3.12)}$$

Equation (S6.3.12) can be used to find values for τ_{PLH} and rise time based upon the times in Fig. S6.3.3. For τ_{PLH}, we require that Eqn. (S6.3.12) satisfies

$$v_O(\tau_{PLH}) = \frac{V_H + V_L}{2} = \frac{V_{DD} - V_{TNL} + V_L}{2}$$

or $$\frac{V_{DD} - V_{TNL} + V_L}{2} = V_{DD} - V_{TNL} - \frac{1}{\dfrac{1}{V_{DD} - V_{TNL} - V_L} + \dfrac{K_L}{2C}\tau_{PLH}} \quad .$$

Solving for t_{PLH} yields

$$\tau_{PLH} = \frac{2C}{K_L}\frac{1}{(V_{DD} - V_{TNL} - V_L)} = \frac{2C}{K_L}\frac{1}{(V_H - V_L)} = 2\,R_{onL}\,C \quad . \qquad \text{(S6.3.13)}$$

where $R_{onL} = \dfrac{1}{K_L(V_{DD} - V_{TNL} - V_L)} = \dfrac{1}{K_L(V_H - V_L)}$ is the on-resistance of the load transistor with $v_{GS} = V_{DD} - V_L$.

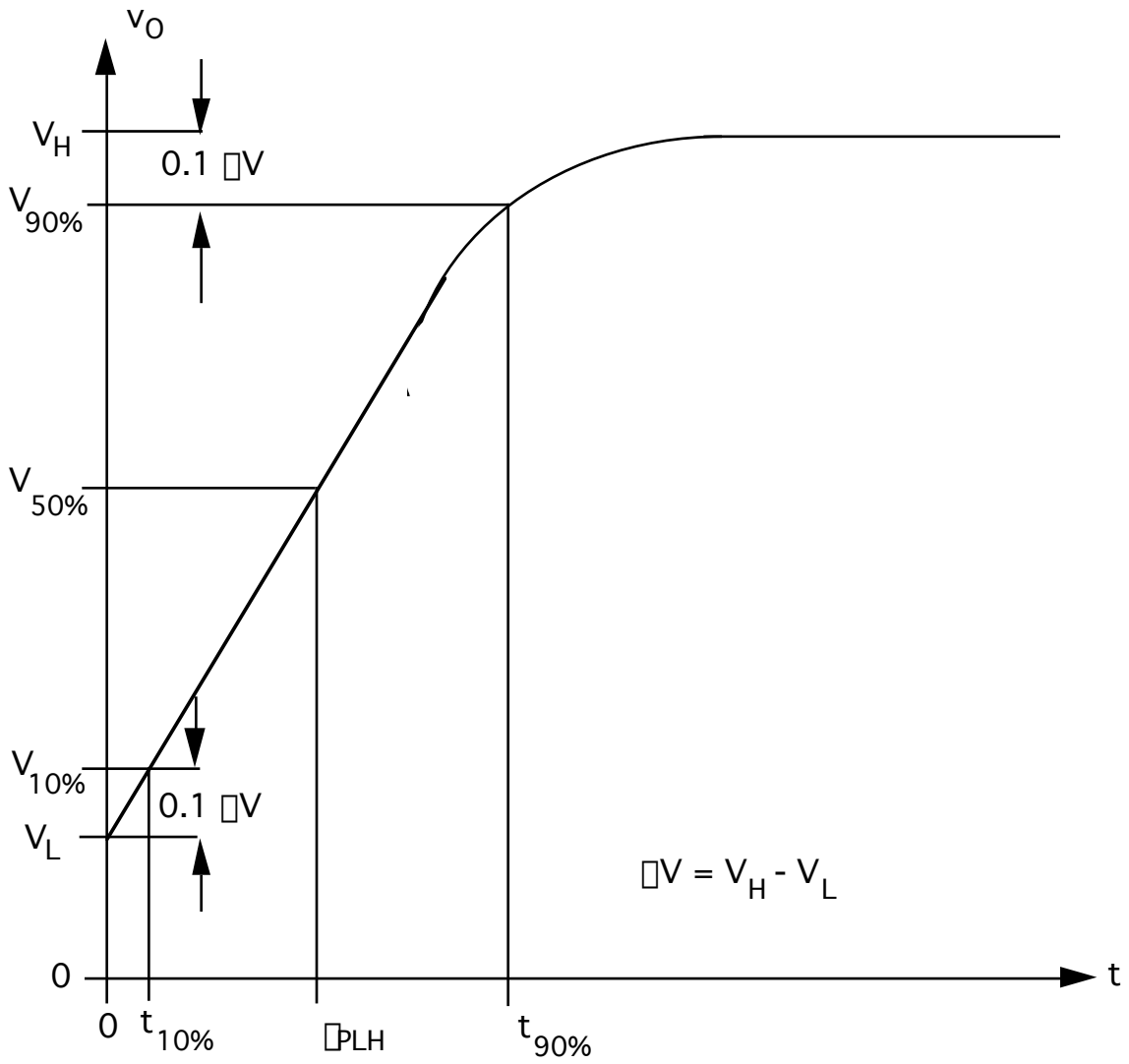

Figure S6.3.3 - Low-to-high switching transient for an inverter with a saturated load device

Rise Time Calculation

In order to find the rise time t_r, we need to calculate the time required for the output to reach the 10% and 90% points on the transition:

$$V_{10\%} = V_L + 0.1\ \Delta V = V_L + 0.1\ (V_H - V_L) = 0.9\ V_L + 0.1\ V_H$$

$$V_{10\%} = 0.9\ V_L + 0.1\ (V_{DD} - V_{TNL})$$

$$V_{90\%} = V_H - 0.1\ \Delta V = V_H - 0.1\ (V_H - V_L) = 0.9\ V_H + 0.1\ V_L$$

$$V_{90\%} = 0.9\,(V_{DD} - V_{TNL}) + 0.1\,V_L\ .$$

Using Eqn. (S6.3.13) to find $t_{10\%}$,

$$\frac{V_H + 9V_L}{10} = V_H - \frac{1}{\dfrac{1}{V_H - V_L} + \dfrac{K_L}{2C}\,t_{10\%}}$$

$$t_{10\%} = \frac{2C}{9K_L}\frac{1}{(V_H - V_L)}\ ,$$

and for $t_{90\%}$

$$\frac{9V_H + V_L}{10} = V_H - \frac{1}{\dfrac{1}{V_H - V_L} + \dfrac{K_L}{2C}\,t_{90\%}}$$

$$t_{90\%} = \frac{18C}{K_L}\frac{1}{(V_H - V_L)}$$

$$t_r = t_{90\%} - t_{10\%} = \frac{160\ C}{9\ K_L}\frac{1}{(V_H - V_L)} = \frac{160}{9}\ R_{onL}\ C \qquad \text{(S6.3.14)}$$

Example S6.3.1: Find τ_{PLH}, τ_{PLH}, t_r and t_f for the inverter with a saturated load from Fig.6.32(b) with a load capacitance C = 0.1 pF.

Solution: For the saturated load inverter with body effect, V_{DD} = 5 V, V_L = 0.25 V, V_L = 3.39V, V_{TNS} = 1 V, K_S = 3.53(25 μA/V^2) and K_L = (25 μA/V^2)/3.39.

Substituting these values into Eqns. (S6.3.7, S6.3.10, S6.3.13 and S6.3.14):

$$\tau_{PHL} = \frac{(0.1\text{pF})}{(3.53)\left(25\,\frac{\mu\text{A}}{\text{V}^2}\right)(3.39 - 1)V}\left[\ln\left(4\,\frac{3.39 - 1}{3.39 + 0.25}\right)(1) + \frac{2(1)}{3.39 - 1}\right] = 0.67\ ns$$

$$t_f = \frac{0.1pF}{(3.53)\left(25\,\frac{\mu A}{V^2}\right)(3.39 - 1)V}\left[\ln\left(\frac{3.39 - 2 + 0.9(3.14)}{3.39 - 0.9(3.14)}\right) + \frac{2}{3.39 - 1}\right] = 1.4\ \text{ns}$$

$$\tau_{PLH} = \frac{2(0.1pF)}{\frac{25}{3.39}\frac{\mu A}{V^2}} \frac{1}{(3.39 - 0.25)V} = 8.6\ ns$$

$$t_r = \frac{160}{9} \frac{(0.1pF)}{\left(\frac{25}{3.39}\frac{\mu A}{V^2}\right)} \frac{1}{(3.39 - 0.25)V} = 77\ ns$$

As expected, we see that τ_{PLH} is an order of magnitude greater than t_{PHL} and also that the rise time is much longer than the fall time. These results are consistent with our assumption that we can neglect the load device current with respect to the switching device current during the high-to-low transition. The rise time is much greater than τ_{PLH} because the pull-up transient takes a long time to approach final value as the saturated load device approaches cutoff.

In summary:

Dynamic Response of the Saturated Load Inverter

$$t_r = t_{90\%} - t_{10\%} = \frac{160}{9}\frac{C}{K_L}\frac{1}{(V_H - V_L)} = \frac{160}{9} R_{onL} C$$

$$t_f = t_4 - t_1 = R_{ons} C \left[\ln\left(\frac{V_H - 2V_{TNS} + 0.9 V}{V_H - 0.9 V}\right) + 2\frac{V_{TNS} - 0.1 V}{V_H - V_{TNS}}\right]$$

$$\tau_{PLH} = \frac{2C}{K_L}\frac{1}{(V_{DD} - V_{TNL} - V_L)} = \frac{2C}{K_L}\frac{1}{(V_H - V_L)} = 2 R_{onL} C$$

$$\tau_{PHL} = t_3 = (t_3 - t_2) + t_2 = R_{ons} C \left[\ln\left(4\frac{V_H - V_{TNS}}{V_H + V_L} - 1\right) + \frac{2V_{TNS}}{V_H - V_{TNS}}\right]$$

$$R_{onL} = \frac{1}{K_L(V_H - V_L)} \quad \text{and} \quad R_{onS} = \frac{1}{K_S(V_H - V_{TNS})}$$